

CLAIMS

What is claimed is:

- 1 1. A method comprising:
 - 2 forming a trench and a via in a layer of dielectric material, the via having one end
 - 3 opening into the trench and an opposing end extending down to a conductor in an
 - 4 underlying layer;
 - 5 selectively depositing a layer of a sacrificial material over the dielectric material layer
 - 6 and over surfaces of the trench and via;
 - 7 depositing a layer of a conductive material over the sacrificial material layer and the
 - 8 conductor in the underlying layer;
 - 9 removing excess conductive material and excess sacrificial material from an upper
 - 10 surface of the dielectric material layer;
 - 11 depositing a layer of a porous dielectric material over the upper surface of the dielectric
 - 12 material layer and exposed portions of the conductive and sacrificial material
 - 13 layers; and
 - 14 removing the sacrificial material to form air gaps surrounding the conductive material
 - 15 within the trench and the via.

- 1 2. The method of claim 1, wherein the sacrificial material layer comprises a
- 2 polymer material.

1 3. The method of claim 2, wherein the sacrificial material layer is deposited
2 using a chemical growth process.

1 4. The method of claim 2, wherein the sacrificial material layer is deposited
2 using a photo induced-free radical polymerization process.

1 5. The method of claim 1, wherein the conductive material comprises copper.

1 6. The method of claim 1, wherein the excess conductive and sacrificial
2 materials are removed from the upper surface of the dielectric material layer using a
3 chemical-mechanical polishing (CMP) process.

1 7. The method of claim 1, wherein the porous dielectric material comprises a
2 silica based material, a silicon nitride based material, a silicon carbide based material, an
3 amorphous carbon based material, or an organic film.

1 8. The method of claim 1, wherein removing the sacrificial material
2 comprises:
3 thermally decomposing the sacrificial material layer into one or more residue materials;
4 and
5 performing a rinse process to remove the residue materials through the porous dielectric
6 layer.

1 9. The method of claim 8, wherein thermal decomposition is performed at a
2 temperature up to approximately 450 °C.

1 10. The method of claim 8, wherein the rinse process is performed using a
2 supercritical CO₂ agent.

1 11. The method of claim 1, wherein the air gaps each have a thickness of
2 between 5 nm and 15 nm.

1 12. The method of claim 1, wherein the underlying layer comprises another
2 layer of dielectric material.

1 13. The method of claim 1, wherein the underlying layer comprises a
2 semiconductor wafer.

1 14. A device comprising:

2 an integrated circuit die; and

3 an interconnect structure disposed over a surface of the die, the interconnect structure

4 including

5 at least a first dielectric layer disposed over the die surface,

6 a number of conductors disposed in the first dielectric layer, at least some

7 of the conductors in electrical communication with conductors of

8 the die,

9 an air gap surrounding at least a portion of each conductor in the first

10 dielectric layer, and

11 a layer of porous dielectric material disposed over at least a portion of the

12 first dielectric layer.

1 15. The device of claim 14, wherein the electrical communication between the

2 conductors in the first dielectric layer and the conductors in the die is formed by a

3 number of conductive vias, at least a portion of each conductive via surrounded by an air

4 gap.

1 16. The device of claim 14, wherein the interconnect structure further
2 comprises:
3 a second dielectric layer disposed over the porous dielectric layer;
4 a number of conductors disposed in the second dielectric layer, at least some of the
5 conductors in electrical communication with conductors in the first dielectric
6 layer; and
7 an air gap surrounding at least a portion of each conductor in the second dielectric layer.

1 17. The device of claim 16, further comprising another layer of the porous
2 dielectric material disposed over at least a portion of the second dielectric layer.

1 18. The device of claim 14, wherein the conductors in the first dielectric layer
2 comprise copper.

1 19. The device of claim 14, wherein the porous dielectric material comprises a
2 silica based material, a silicon nitride based material, a silicon carbide based material, an
3 amorphous carbon based material, or an organic film.

1 20. The device of claim 14, wherein the air gaps each have a thickness of
2 between 5 nm and 15 nm.

1 21. A system comprising:

2 a memory; and

3 a processing device coupled with the memory, the processing device including an

4 integrated circuit die and an interconnect structure disposed over a surface of the

5 die, the interconnect structure including

6 at least a first dielectric layer disposed over the die surface,

7 a number of conductors disposed in the first dielectric layer, at least some

8 of the conductors in electrical communication with conductors of

9 the die,

10 an air gap surrounding at least a portion of each conductor in the first

11 dielectric layer, and

12 a layer of porous dielectric material disposed over at least a portion of the

13 first dielectric layer.

1 22. The system of claim 21, wherein the electrical communication between

2 the conductors in the first dielectric layer and the conductors in the die is formed by a

3 number of conductive vias, at least a portion of each conductive via surrounded by an air

4 gap.

1 23. The system of claim 21, wherein the interconnect structure further
2 comprises:
3 a second dielectric layer disposed over the porous dielectric layer;
4 a number of conductors disposed in the second dielectric layer, at least some of the
5 conductors in electrical communication with conductors in the first dielectric
6 layer; and
7 an air gap surrounding at least a portion of each conductor in the second dielectric layer.

1 24. The system of claim 23, further comprising another layer of the porous
2 dielectric material disposed over at least a portion of the second dielectric layer.

1 25. The system of claim 21, wherein the conductors in the first dielectric layer
2 comprise copper.

1 26. The system of claim 21, wherein the porous dielectric material comprises
2 a silica based material, a silicon nitride based material, a silicon carbide based material,
3 an amorphous carbon based material, or an organic film.

1 27. The system of claim 21, wherein the air gaps each have a thickness of
2 between 5 nm and 15 nm.

1 28. A method comprising:

2 forming a trench and a via in a layer of dielectric material, the via having one end

3 opening into the trench and an opposing end extending down to a conductor in an

4 underlying layer;

5 depositing a layer of a sacrificial material over the dielectric material layer and over

6 surfaces of the trench and via;

7 etching the sacrificial material layer to remove at least a portion of the sacrificial material

8 layer overlying the conductor in the underlying layer;

9 depositing a layer of a conductive material over the sacrificial material layer and the

10 conductor in the underlying layer;

11 removing excess conductive material and excess sacrificial material from an upper

12 surface of the dielectric material layer;

13 depositing a layer of a porous dielectric material over the upper surface of the dielectric

14 material layer and exposed portions of the conductive and sacrificial material

15 layers; and

16 removing the sacrificial material to form air gaps surrounding the conductive material

17 within the trench and the via.

1 29. The method of claim 28, wherein the sacrificial material layer comprises a

2 polymer material.

1 30. The method of claim 28, wherein the conductive material comprises
2 copper.

1 31. The method of claim 28, wherein the porous dielectric material comprises
2 a silica based material, a silicon nitride based material, a silicon carbide based material,
3 an amorphous carbon based material, or an organic film.

1 32. The method of claim 28, wherein removing the sacrificial material
2 comprises:
3 thermally decomposing the sacrificial material layer into one or more residue materials;
4 and
5 performing a rinse process to remove the residue materials through the porous dielectric
6 layer.

1 33. The method of claim 28, etching the sacrificial material layer to remove at
2 least a portion of the sacrificial material layer overlying the conductor in the underlying
3 layer comprises performing an anisotropic etch process.